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DATA FLOW ORIENTED HARDWARE DESIGN OF RNS-BASED POLYNOMIAL MULTIPLICATION FOR SHE ACCELERATION

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IMPLEMENTATION PROBLEMATIC FOR RLWE-BASED LEVELED-FHE SCHEMES

- **Handling polynomial of $\boldsymbol{R} = \mathbb{Z}[X]/(F(X))$ and $\boldsymbol{R}_q = \boldsymbol{R}/q\boldsymbol{R}$:**
  - Modulus q ~ several hundred of bits
  - deg(F) ~ several thousand

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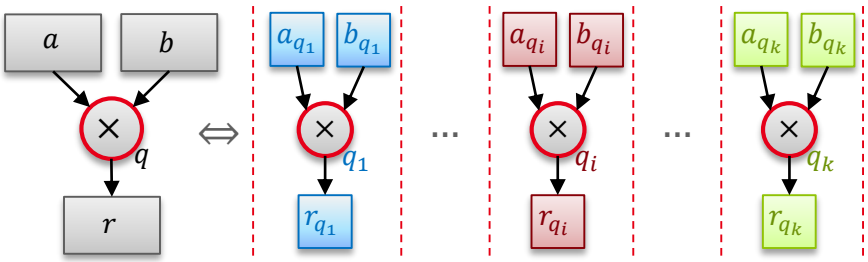

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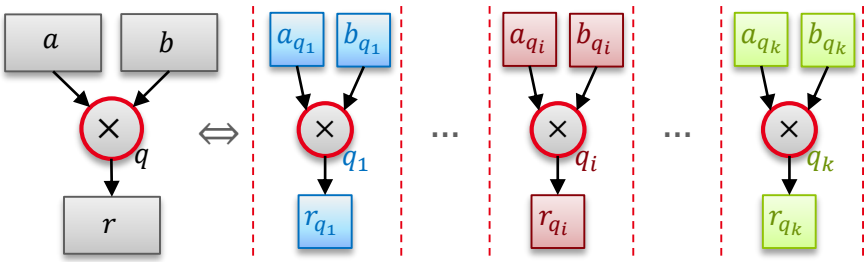

- **Bajard et al. in 2016, further simplified by Halevi et al. in 2018 :**
  - RNS compatible $\mathrm{FV.Dec}_{RNS}$ and $\mathrm{FV.Mult\&Relin}_{RNS}$.
  - New $\boldsymbol{rlk}_{RNS}$: pair of $k \times k$–matrices with elements in R_{q_i} for i in $1, \ldots, k$.
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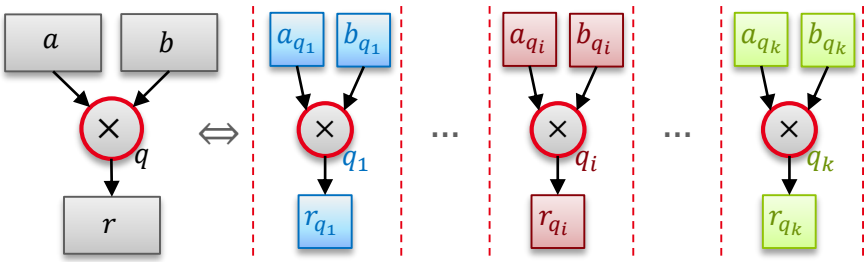

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- **Negative Wrapped Convolution over $R_{q_i} = \mathbb{Z}_{q_i}[X]/(F(X))$:**
  - No polynomial modular reduction.
  - Restrict the choice of $F(X) = X^n + 1$ with n a power of 2.
  - Restrict the choice of q_i: $q_i \equiv 1 \bmod 2n$.
  - $2nk$ precomputed values: $(\psi_i^j)_{0 \le j < 2n}$, where ψ_i a n-th primitive root of -1 in $\mathbb{Z}_{q_i}^*$.

RELATED WORKS (HARDWARE ACCELERATION)

- **Migliore et al. 2018: Karatsuba rather than NWC (no RNS)**
  - Finer choice of $F(X)$ allowing batching of binary messages.
  - Asymptotic complexity in $O(n^{1,585})$ Vs $O(n \log n)$: turning point ($n = 6144$, $\log_2 q = 512$).

  Not sufficient to target large multiplicative depth.

- **Öztürk et al. 2015: RNS and NTT approach for LTV scheme (no NWC)**
  - Memory-access iterative NTT.
  - External pre-computation of NTT twiddle factors.

  Use communication bandwidth for non-payload data.

- **Cousins et al. 2017: RNS and NTT approach for LTV scheme**
  - Dataflow oriented pipelined NTT.
  - Local storage of all twiddle factors at compile time.

  Storage cost in O(kn), dependent of RNS basis size.

- **Sinha Roy et al. 2015: RNS and NTT (no NWC) approach for RLWE-based scheme**
  - Memory-access iterative NTT.
  - Local storage of a subset of the twiddle factors, and computation on-the-fly of the others.

  Better storage in O($k \log n$), but still dependent of RNS basis size.

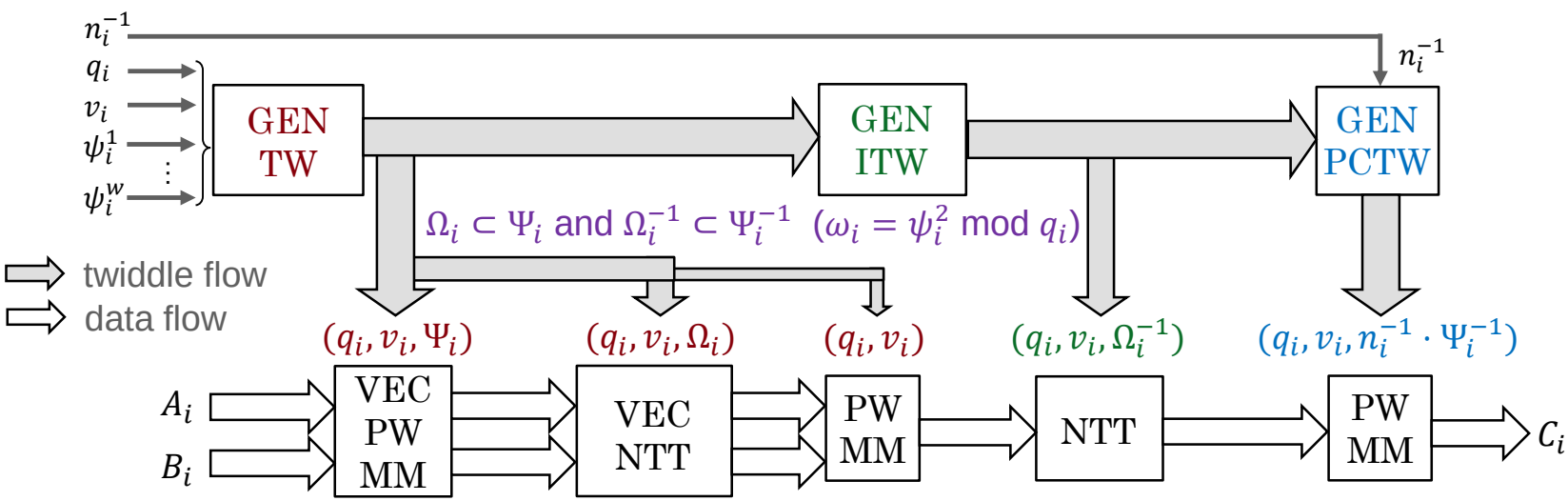
Dataflow oriented NWC with on-the-fly computation of twiddle factors

NWC ARCHITECTURE PRINCIPLE

- **Architecture principle:**

  One NWC over $\boldsymbol{R} \Leftrightarrow O(k)$ smaller NWC over the $\boldsymbol{R}_{q_i}$'s : $C_i = \mathrm{NWC}_i(A_i, B_i)$

- **Required values for NWC_i:**
  - ψ_i: a n-th primitive root of -1 over $\mathbb{Z}_{q_i}^* \Rightarrow \omega_i = \psi_i^2$ mod q_i is a n-th primitive root of 1 over $\mathbb{Z}_{q_i}^*$



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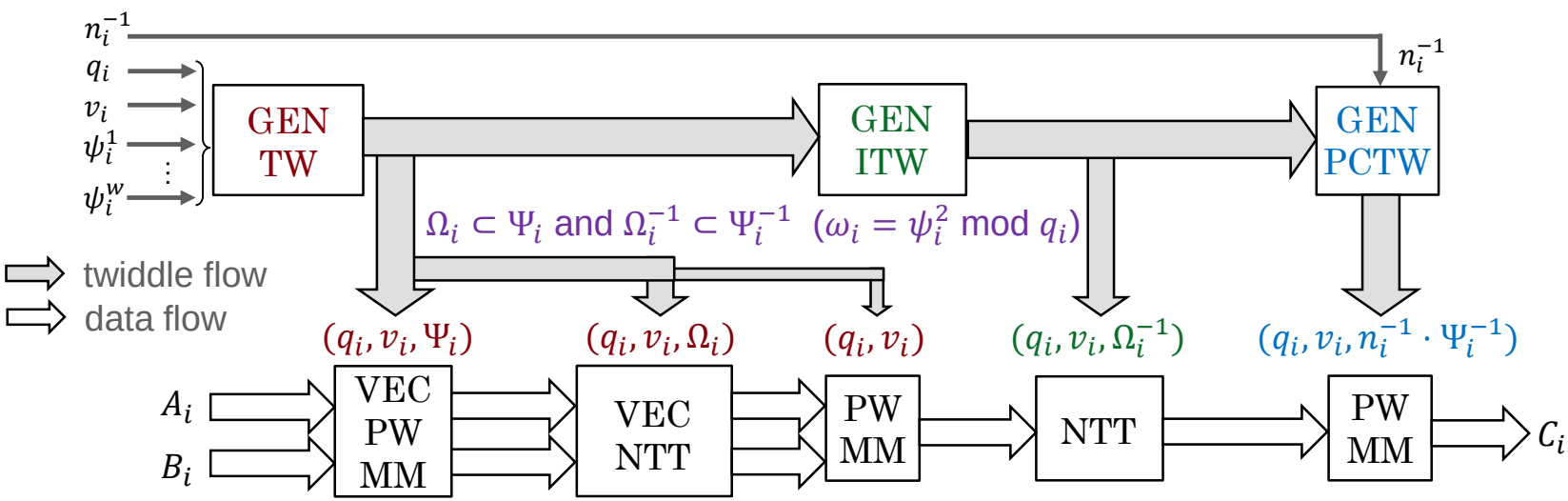
$O(w)$ seeds $\ll O(n)$ twiddles

Generation of $\Psi_i = \left(\psi_i^j\right)_{j=0}^{n-1}$.

One set every $T = \frac{n}{w}$ cycles.



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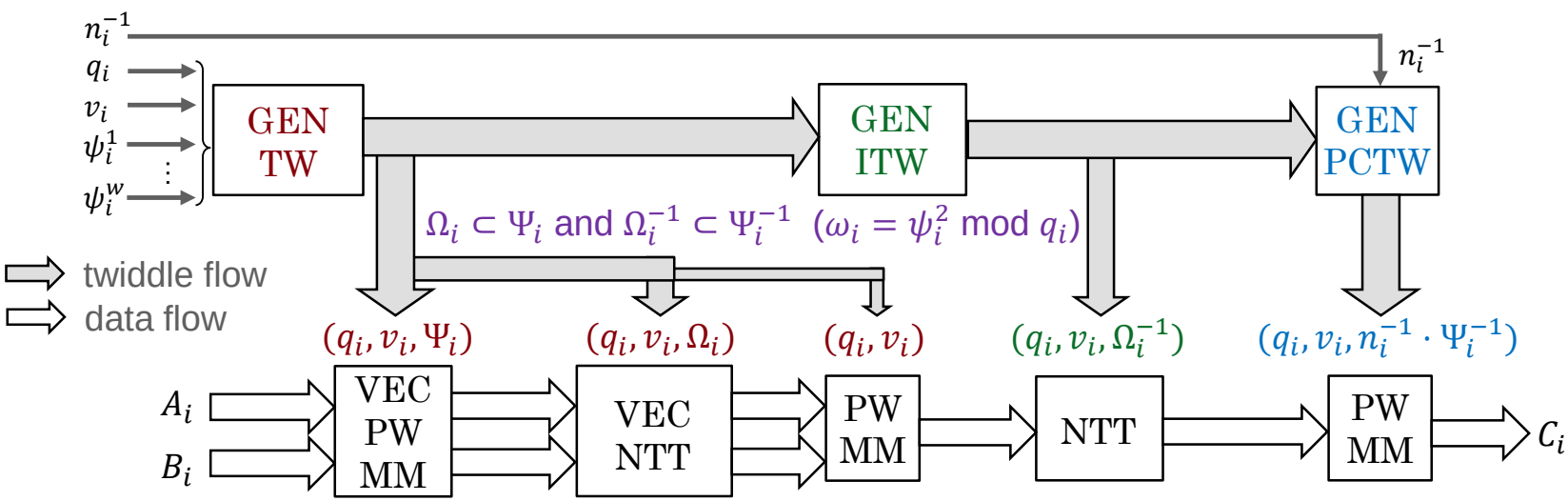

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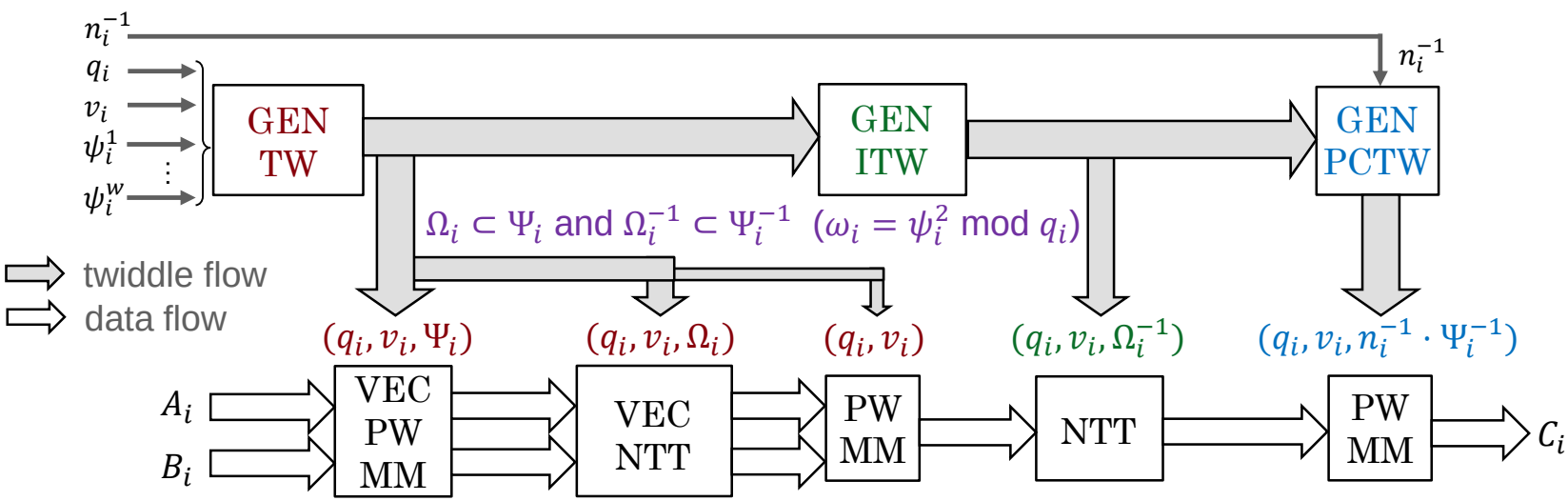

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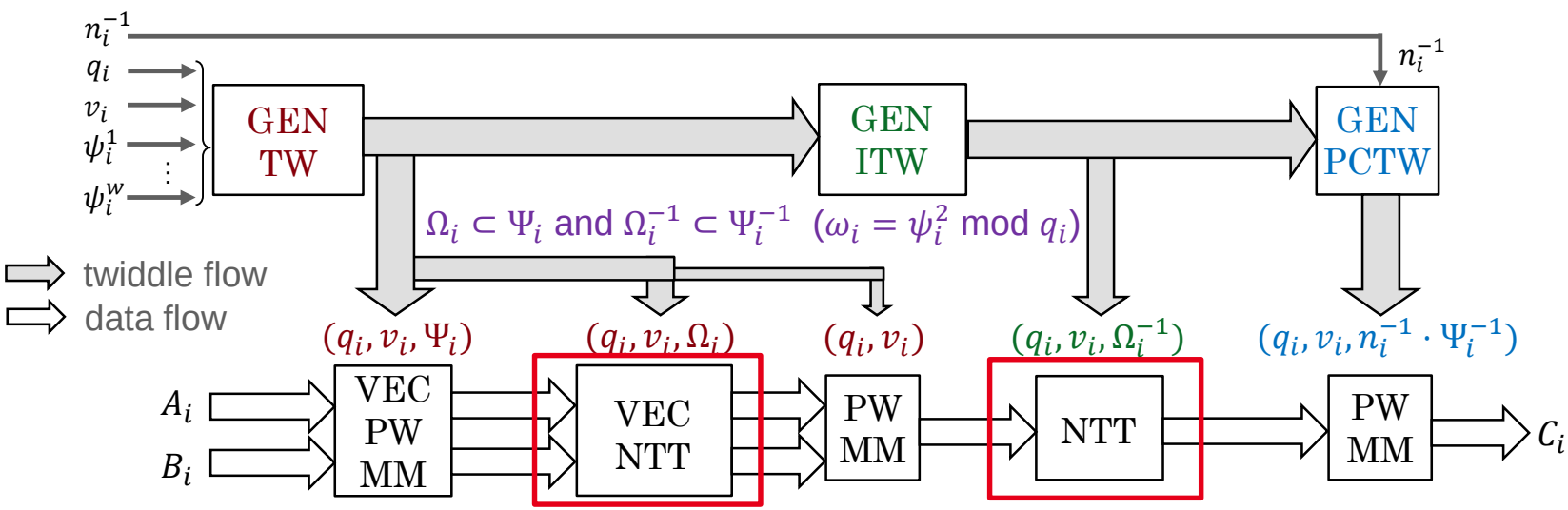

AUTOMATIC GENERATION OF MULTI FIELD NTT DESIGN (1)

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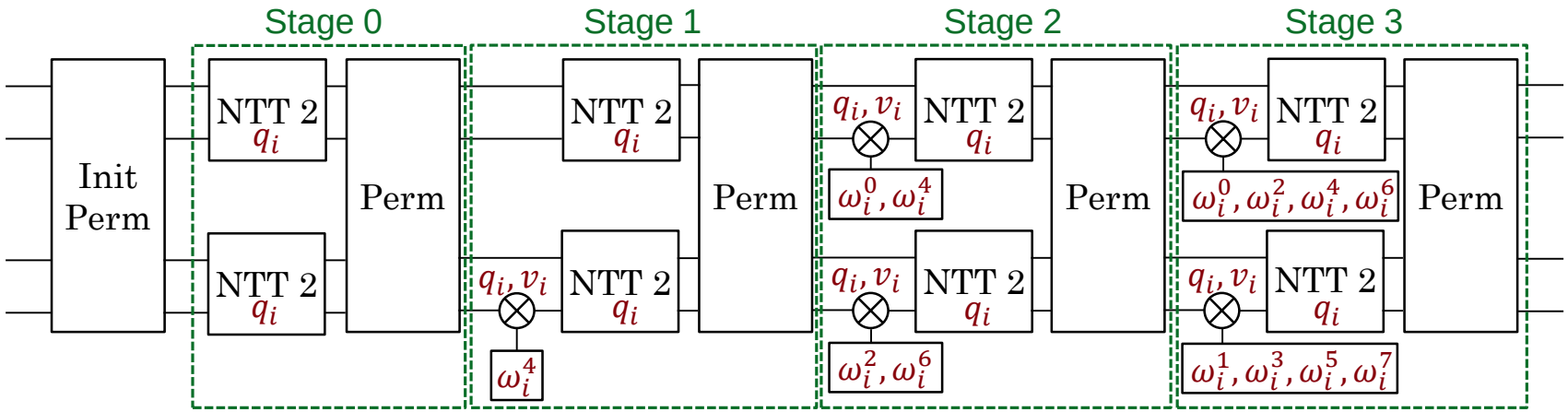

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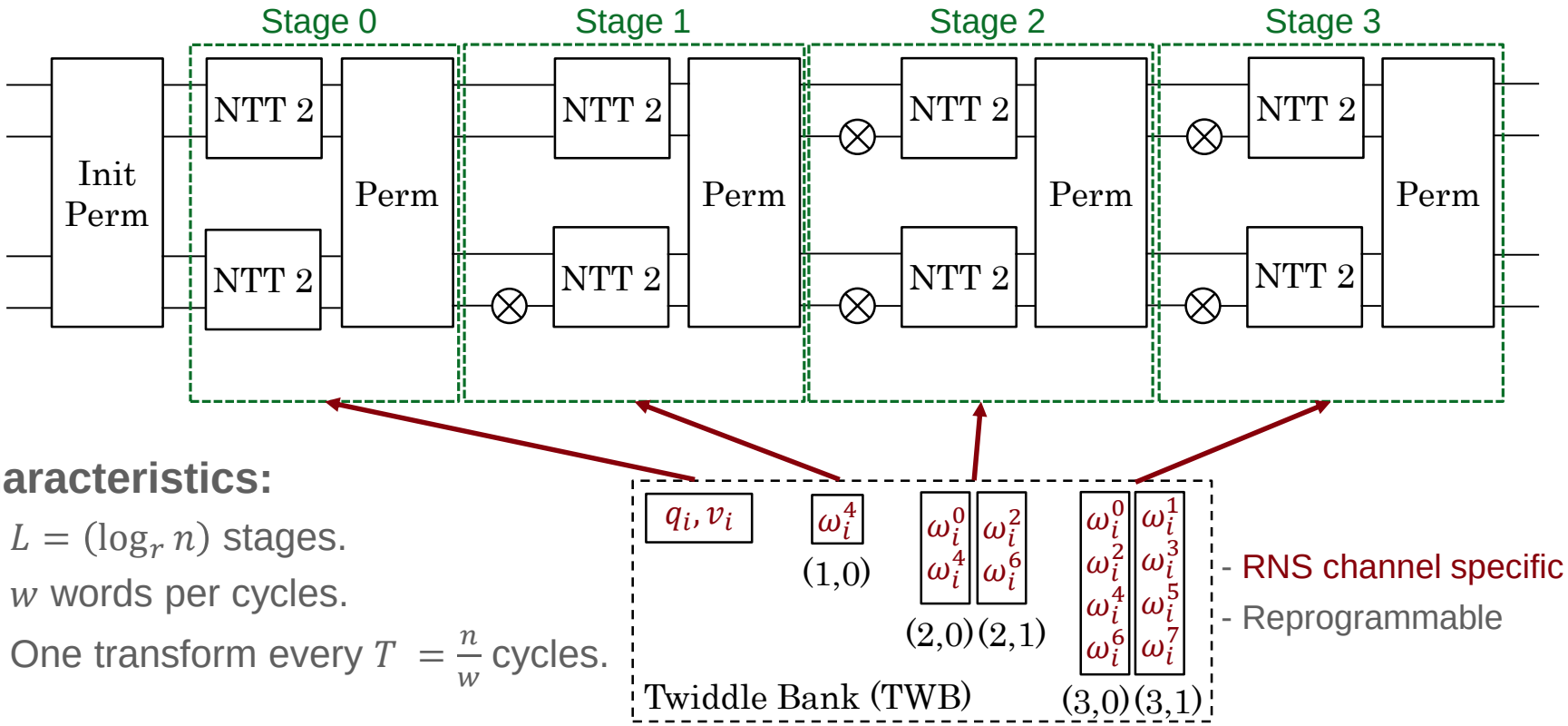

- RNS channel specific
- Reprogrammable

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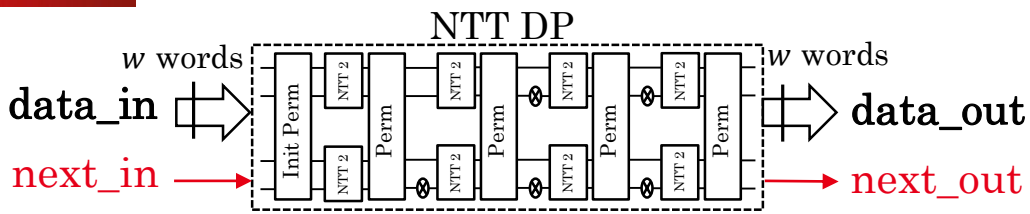

- twiddle flow
- read addresses
- write addresses
- write enables

l : stage index

t : way index (in $0, \dots, \frac{w}{2} - 1$)

Cyclic access and reprogramming of TWB

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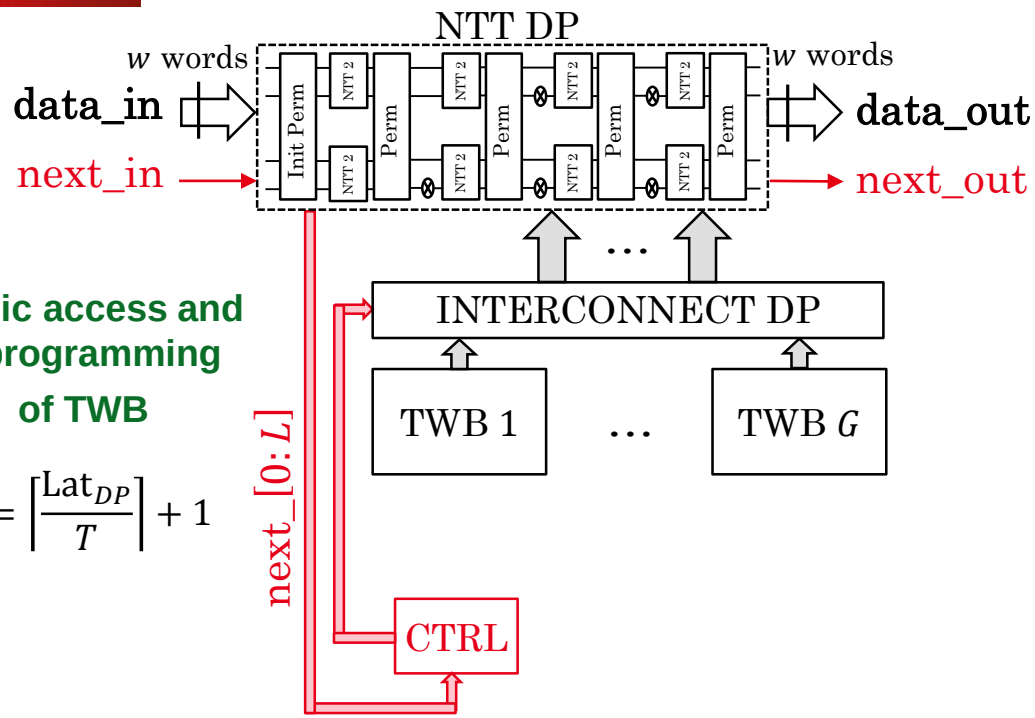

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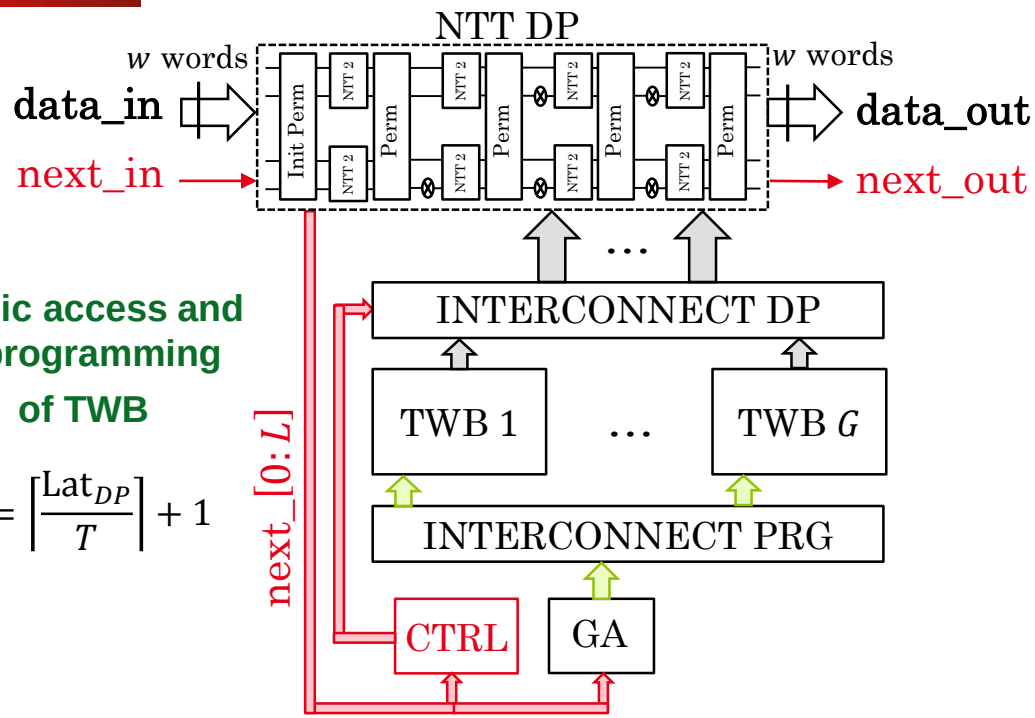

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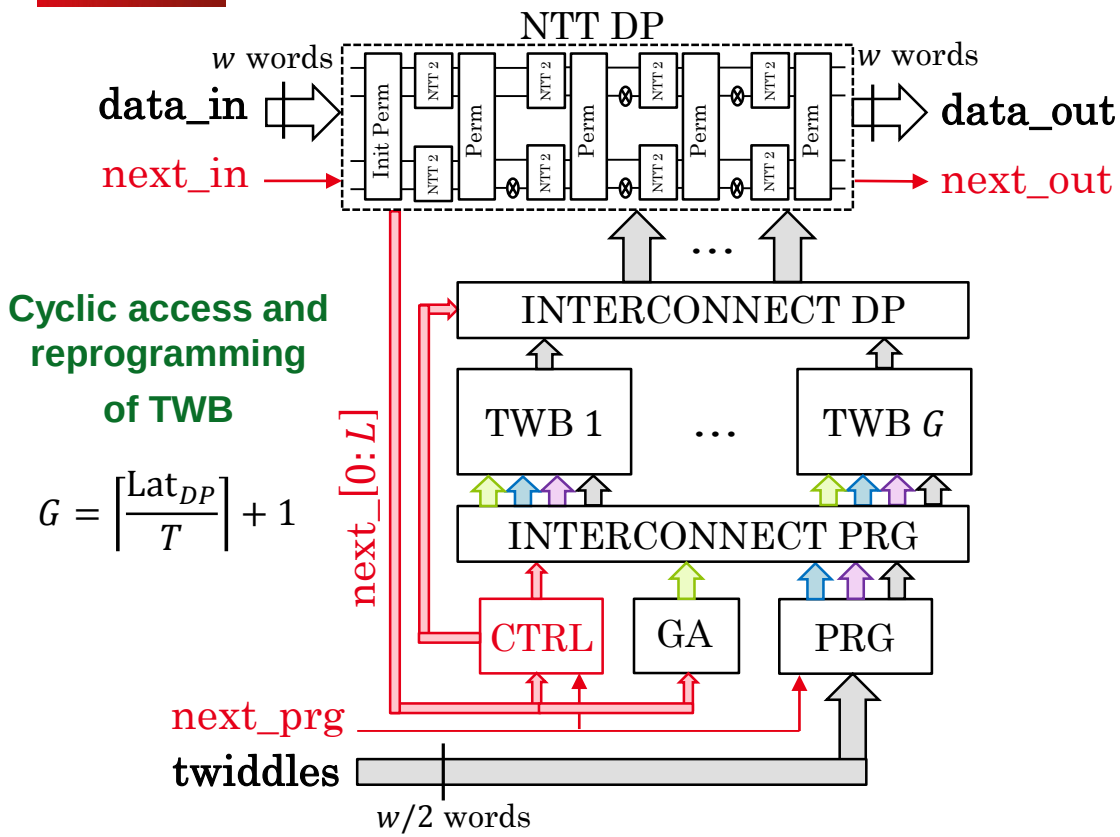

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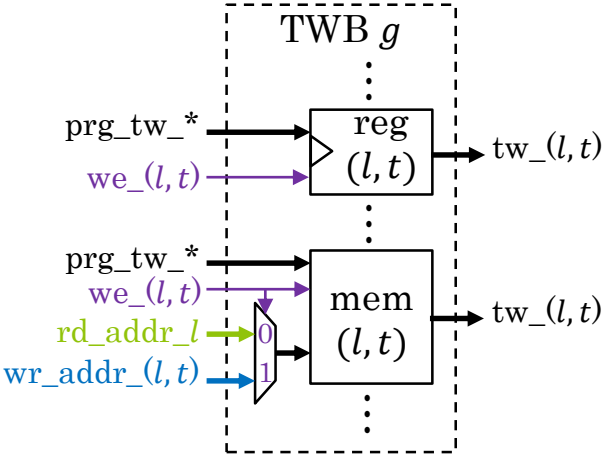

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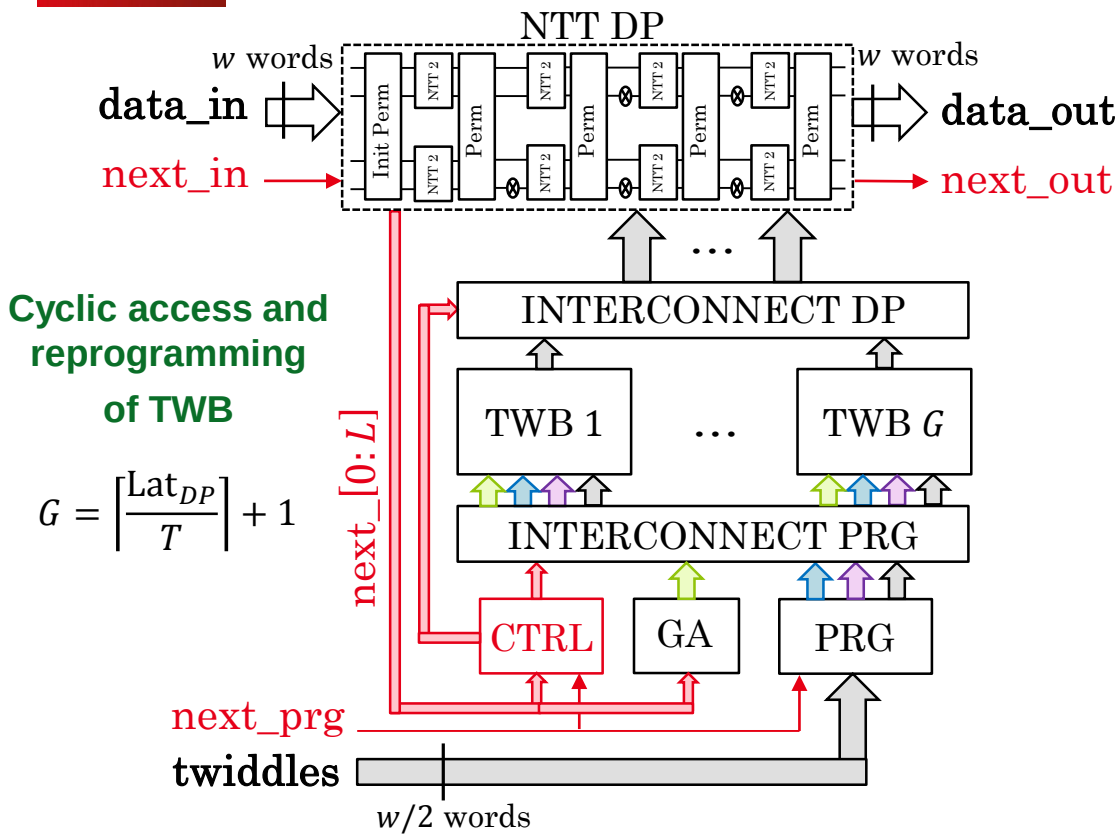

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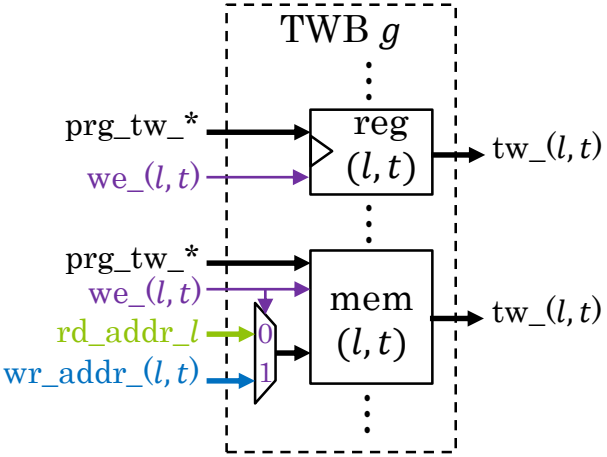


- **Example of reprogram counters ($r = 2$, $n = 16$, $w = 4$):**

twiddles ⇒ $w/2$ words per cycles

Select from the flow ⇒ Update $\mathrm{we\_}(l,t)$ and $\mathrm{wr\_addr\_}(l,t)$

prg_tw_0 ⟶ $\omega_i^0, \omega_i^2, \omega_i^4, \omega_i^6$

prg_tw_1 ⟶ $\omega_i^1, \omega_i^3, \omega_i^5, \omega_i^7$

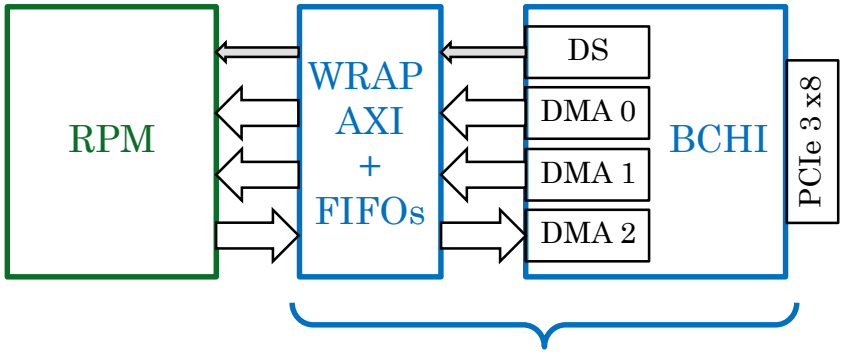
Counter for mem(2,1) : offset 1, step 2, index 0 $\boxed{\omega_i^2, \omega_i^6}$

Counter for mem(3,1) : offset 0, step 1, index 1 $\boxed{\omega_i^1, \omega_i^3, \omega_i^5, \omega_i^7}$

RPM CHARACTERIZATION
PROOF-OF-CONCEPT INTEGRATION (1)

- **Preliminary integration:**
  - Alpha-Data ADM-PCIE 7v3.
  - Xilinx Virtex 7: XC7VX690T-2-FFG1157C.
  - PCIe Gen3, 8 lanes.
  - Vivado 2016.3: placed and routed.

$f_{RPM} = 200$ MHz



$n = 2^{12}$, $\log q_i = 30$, $w = 2$

Ressources		RPM					BCHI
type	available	total	NTT	MM	GTW	Others	& WRAP
LUT	432,368	**54,188**	41,964	5,198	5,906	1,120	27,775
LUTRAM	173,992	**14,402**	10,710	2,056	1,550	86	5,425
FF	864,736	**66,444**	50,961	6,755	7,761	967	39,614
BRAM	1,470	**208**	147	0	21	40	153
DSP	3,600	**517**	363	88	66	0	48
IO	600	**0**	0	0	0	0	59
Pcie	3	**0**	0	0	0	0	1

LUT	12.5%
LUTRAM	8.3%
FF	7.7%
BRAM	**14.1%**
DSP	**14.4%**

LUT	6.4%
LUTRAM	3.1%
FF	4.6%
BRAM	10.4%
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Test PCIe Ok!

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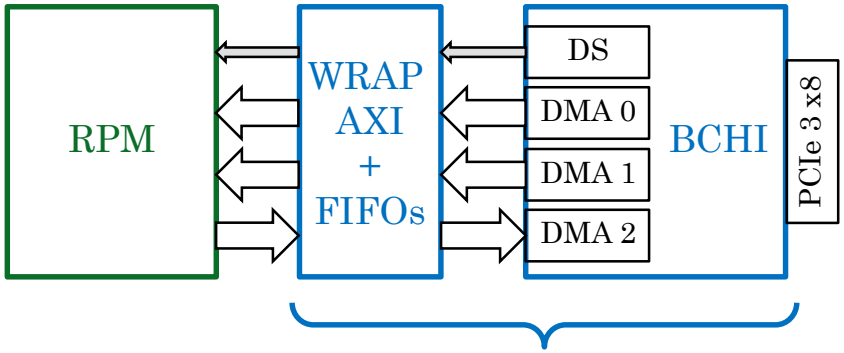

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RPM more constraining resources:

- BRAM slices
- DSP slices
- PCIe bandwidth

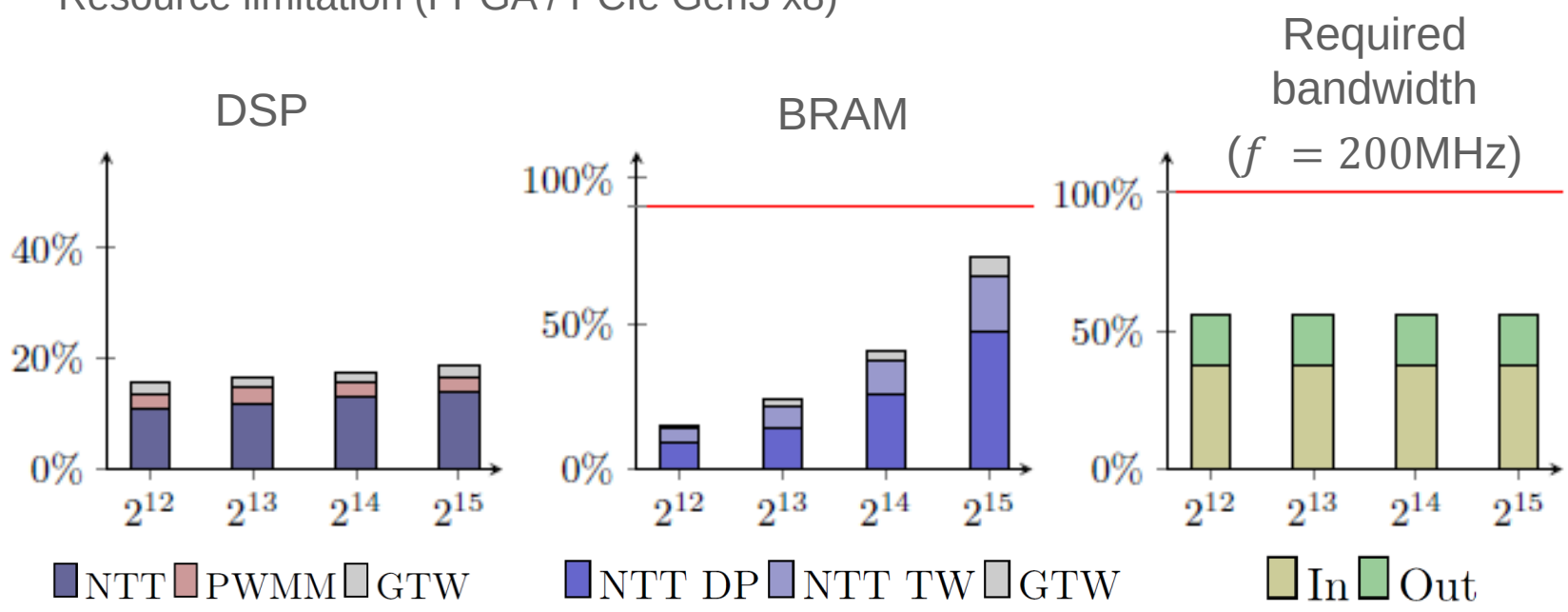
How does RPM scale in SHE context?

RPM CHARACTERIZATION PROJECTIONS (1)

- **Impact of the polynomial degree** n ($w = 2$ and $\log_2 q_i = 30$)**:**

Xilinx Virtex 7: XC7VX690T-2-FFG1157C

— Resource limitation (FPGA / PCIe Gen3 x8)



Slight increase in DSP utilization.

BRAM is restrictive for $n > 2^{15}$ ([58-65]% for NTT permutations)

Required bandwidth is acheivable

RPM CHARACTERIZATION PROJECTIONS (2)

- **Impact of the streaming width** w ($n = 2^{14}$ and $\log_2 q_i = 30$):

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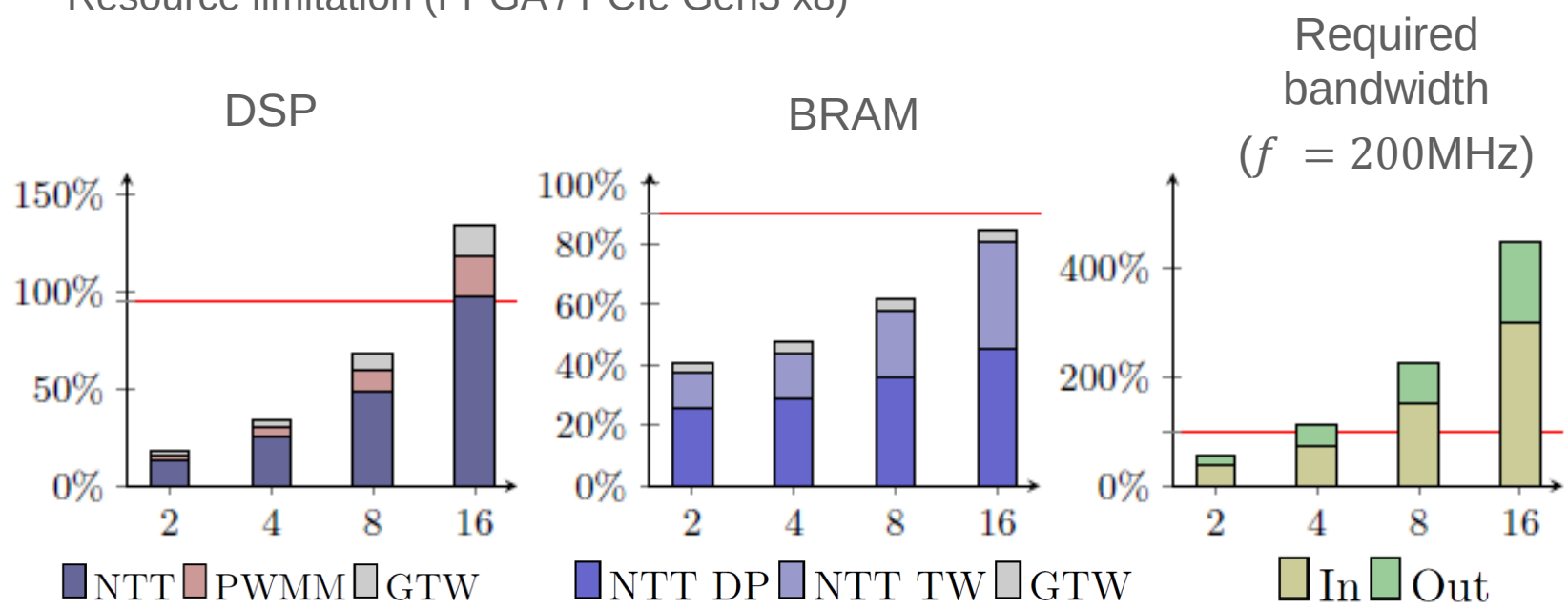


Great increase in DSP utilization.

Increase of BRAM utilization.

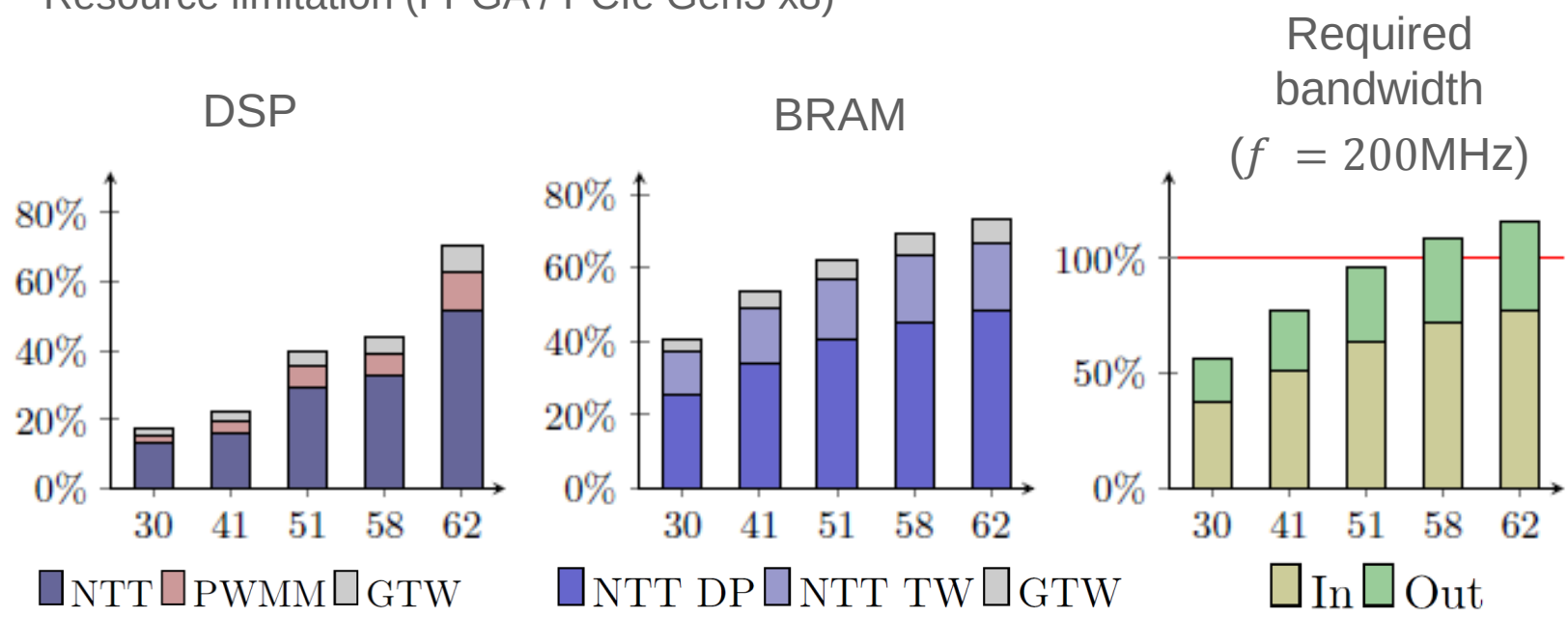
Required bandwidth is prohibitive

RPM CHARACTERIZATION PROJECTIONS (3)

- **Impact of the RNS prime size** $\log_2 q_i$ ($n = 2^{14}$ and $w = 2$)**:**

Xilinx Virtex 7: XC7VX690T-2-FFG1157C

— Resource limitation (FPGA / PCIe Gen3 x8)



Balanced impact on DSP and BRAM utilization.

Required Bandwidth may become restrictive.

PERFORMANCE PROJECTIONS: FV-RNS APPLICATION

- **Raw performances:**

RPM / s $\frac{f_{RPM}}{\frac{n}{w}}$

Required bandwidth $\sim f_{RPM} 3w \log_2 q_i$

- **Performance projection @200MHz:**

With respect to timing from [HPS18] ($\lambda > 128$)

Parameters						RPM	Mul.RPM		Relin.RPM		Total	BW
L	n	S_q	s	k	w	1/ms	$3(k+k')$	ms (**su**)	$2k^2$	ms (**su**)	ms (su)	GB/s
1	2^{12}	94		4		97.7	27	0.3 (**37.3**)	32	0.3 (**5.1**)	6.3 (2.8)	4.5
5	2^{13}	141		5		48.8	33	0.7 (**44.7**)	50	1.0 (**6.9**)	18.2 (3.0)	4.5
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					16	195.3		0.4 (**387**)		1.7 (**50.3**)	104.2 (3.4)	36
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Increasing prime size:

- Slightly improves speedup.
- Balanced cost on DSP and BRAM usage.
- Bandwidth may be restrictive.

CONCLUSION & PERSPECTIVES

- **Hardware implementation for SHE should be flexible:**
  - Refinement of parameter range still in progress.
  - Multiplicative depth has significant impact on both n and $\log_2 q$.

- **Our response:**
  - Dataflow RNS-based NWC with on-the-fly generation of twiddles.
  - Exploiting DSP knowledge on DFT implementation.
  - Minimize the impact of $\log_2 q$ on hardware design.

- **Research perspectives:**
  - NTT Vs RPM?
  - Proper system integration
  - Design space exploration with SPIRAL

- **Application perspectives:**
  - Hybrid architecture for SHE acceleration

Thanks!

Questions?

Centre de Saclay
Nano-Innov PC 172 - 91191 Gif sur Yvette Cedex

INTRODUCTION : HOMOMORPHIC ENCRYPTION

- **Decryption function is an homomorphism:**

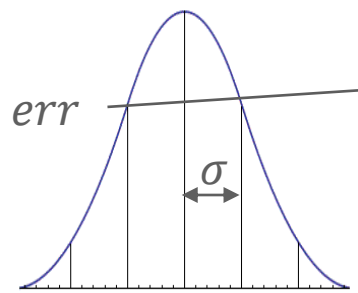
c_1, c_2 two ciphertexts such that $c_1 = \mathrm{Enc}(m_1)$ and $c_2 = \mathrm{Enc}(m_2)$ $\Rightarrow$ $\begin{cases} \mathrm{Dec}(c_1) \circ \mathrm{Dec}(c_2) = \mathrm{Dec}(c_1 \circledcirc c_2) \\ m_1 \circ m_2 \Leftrightarrow c_1 \circledcirc c_2 \end{cases}$

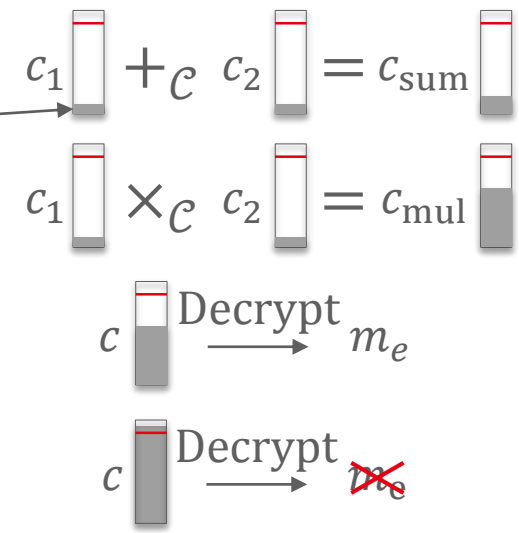
- **Semantic security : noise in ciphertexts**

$m \in \mathcal{M}$ message space

$m_e \in \mathcal{H}$ cleartext space

$c \in \mathcal{C}$ ciphertext space





$m \xrightarrow{\mathrm{Encode}} m_e \xrightarrow{\mathrm{Encrypt}} c$

$c \xrightarrow{\mathrm{Decrypt}} m_e \xrightarrow{\mathrm{Decode}} m$

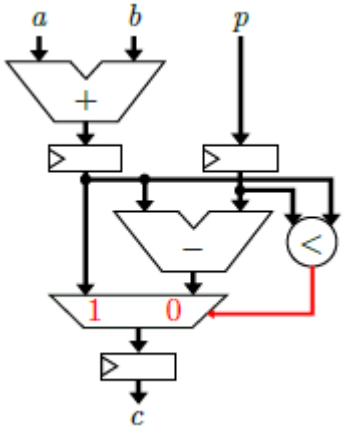
Error distribution χ_{err}

Usually $\chi_{err} = N(0, \sigma^2)$

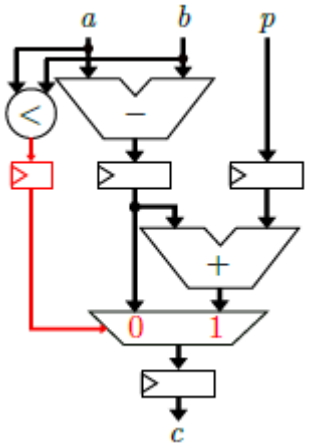
Homomorphic encryption has to be secure … <u>and correct</u> !

MODULAR ARITHMETIC

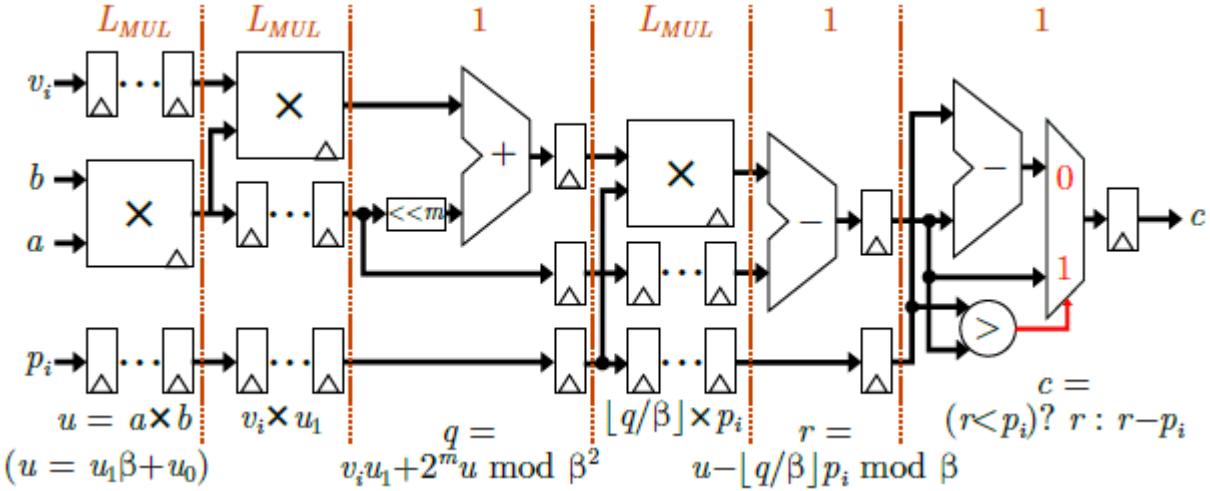
- **Modular Addition:**



- **Modular Subtraction:**

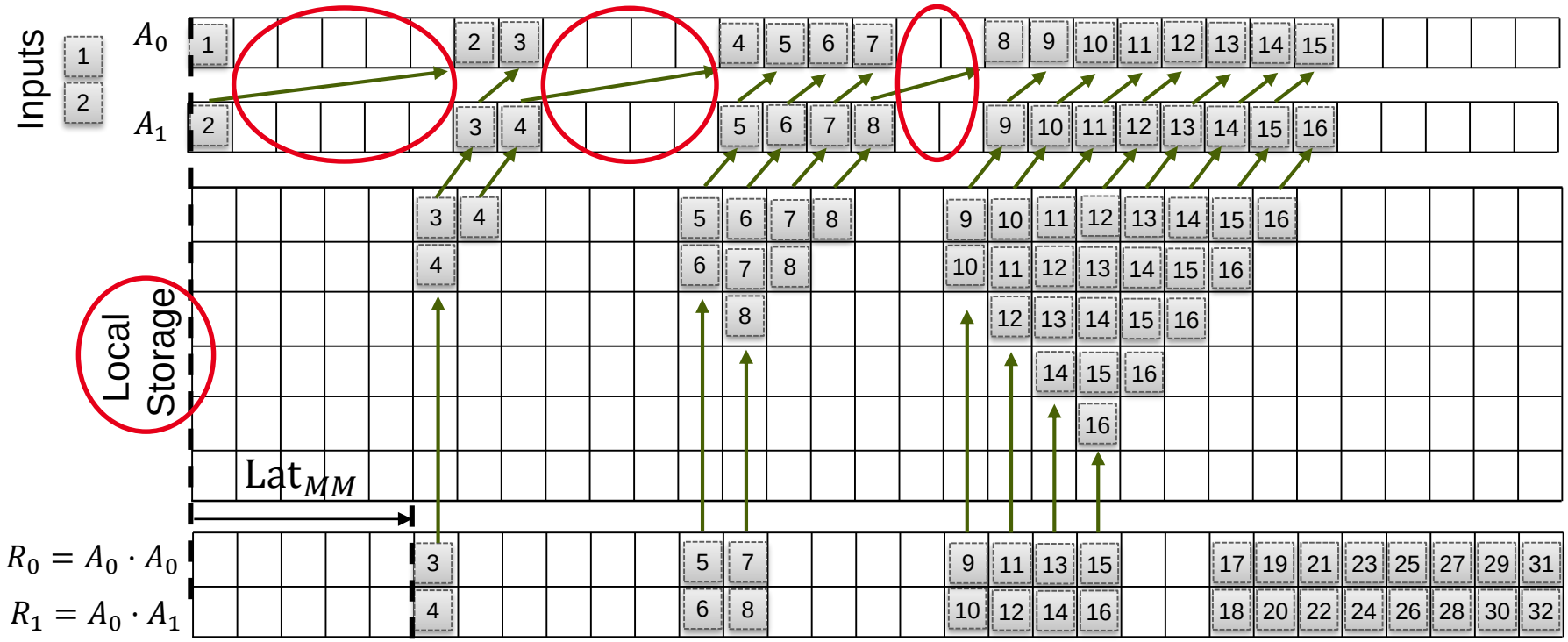


- **Modular Multiplication (NFLlib):**



GENERATION OF TWIDDLE FACTORS (1)

- **Problematic of twiddle generation:**
  - Data dependencies.
  - Modular multiplication latency.
  - Required throughput $T = \frac{n}{w}$.
- **Example of recurrence relation:**
  - $\psi^{2k} = \psi^k \cdot \psi^k$ and $\psi^{2k+1} = \psi^k \cdot \psi^{k+1}$
  - Intermediate storage in $O\left(\frac{n}{4}\right)$
  - Compute "at the earliest"
- **Example of Ψ generation ($n = 32$, $w = 2$):**



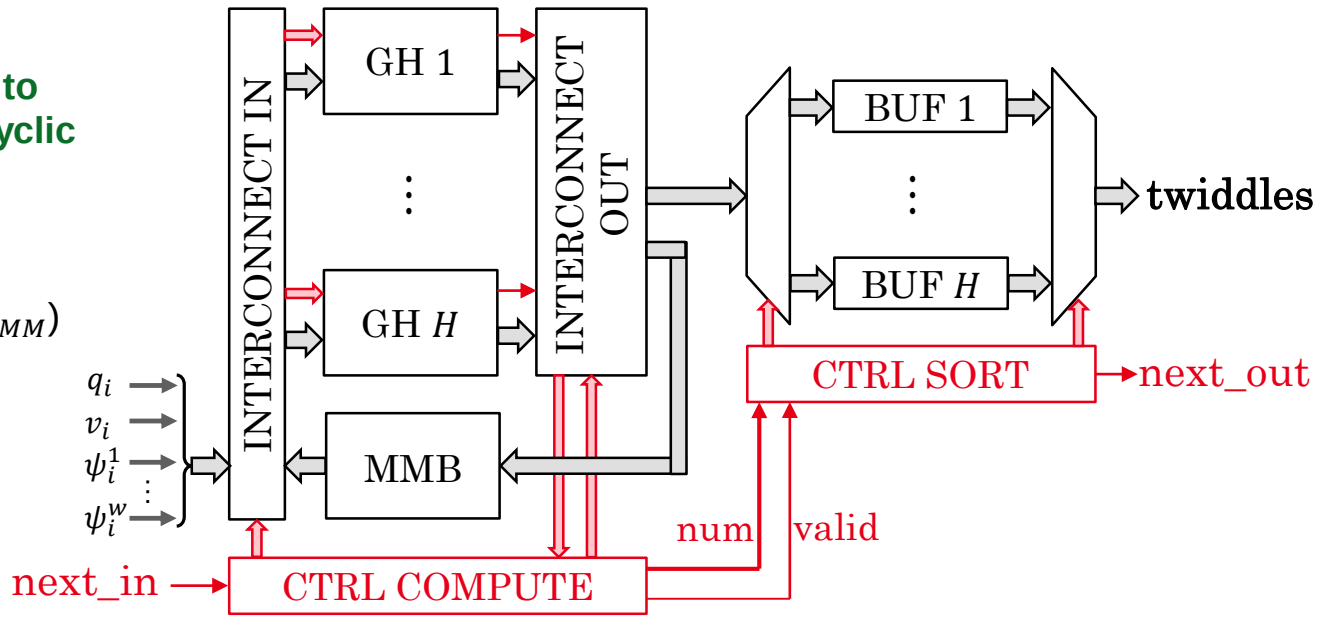
GENERATION OF TWIDDLE FACTORS (2)

- **Data flow twiddle generation:**

Sequential access to MMB (w MMs) with cyclic priority order

$$H = \left\lceil \frac{\mathrm{Lat}_{GEN}}{T} \right\rceil + 1$$

$(H = 3 \text{ when } T \gg \mathrm{Lat}_{MM})$



- **Minimize Generation Handler local storage:**

$$\mathrm{bunch}_t \begin{cases} \psi^{t+1} \\ \psi^{t+2} \\ \vdots \\ \psi^{t+w} \end{cases}$$

$$\text{twiddle set} \approx (\mathrm{bunch}_t)_{t=0}^{T-1}$$

$$f_j = \psi^{jw}$$

$$\mathrm{bunch}_{t_{next}} = f_j \cdot \mathrm{bunch}_{t_{last}}$$

$$(t_{next} = j + t_{last})$$

j is upper bounded by design parameter only

$\Downarrow$

Local storage independent of n!